CIRCUIT FOR DETECTING THE LOCKED CONDITION OF PSK OR QAM

This application is a continuation of application Ser. No. 08/675.632. filed Jul. 1. 1996. entitled A CIRCUIT FOR DETECTING THE LOCKED CONDITION OF PSK AND QAM DEMODULATORS. now U.S. Pat. No. 5.703.526.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to PSK (Phase-Shift Keying) and QAM (Quadrature Amplitude Modulation) modulation techniques for simultaneously transmitting a plurality of bits. The present invention more particularly relates to the detection of the locked condition of PSK or QAM demodulators.

2. Discussion of the Related Art

FIG. 1 schematically represents a conventional QPSK (Quadrature PSK) demodulator. Such a QPSK demodulator is used to extract from a signal Sm two binary signals I and Q modulated in phase quadrature. Signal Sm is generally expressed by I cos ωt+Q sin ωt. where cos ωt and sin ωt are two carriers having the same frequency ω/2π. but are in phase quadrature. Signal Sm is applied to two multipliers **10** and **11** which further receive signal cos ωt and signal sin ω. respectively. provided by a voltage controlled oscillator (VCO) **13** connected in a phase-locked loop (PLL). If the frequency of oscillator **13** is close to the frequency of the carrier. multiplier **10** provides a signal having a mean value corresponding to signal I and an a.c. component whose frequency is twice the carrier's frequency. Similarly. multiplier **11** provides a signal having a mean value corresponding to signal Q and an a.c. component whose frequency is twice the carrier's frequency. Low-pass filters **15** eliminate the a.c. components of the outputs of multipliers **10** and **11** and respectively provide signals I and Q.

A phase detector **17** receives signals I and Q and provides a signal φ indicative of the phase error of signals I and Q. Signal φ controls the frequency of oscillator **13** so that the phase difference φ tends to zero. Generally, signal φ is applied to oscillator **13** through a low-pass filter **19** whose cut-off frequency is very low so that oscillator **13** is only controlled by the mean variations of signal φ.

FIG. 2A illustrates a conventional representation. in the form of a "constellation". of the possible combinations of the demodulated binary signals I and Q. The values of signal I are read along a horizontal axis I. and the values of signal Q are read along a vertical axis Q. In QPSK modulation. each signal I and Q has a positive value or a negative value of the same amplitude. corresponding to the high and low logic levels. The nominal constellation. corresponding to the case where the signals provided by oscillator **13** are in phase with the two carriers in quadrature. includes four points P1-P4 that are symmetrical with respect to axes I and Q.

When the signals of oscillator **13** are phase shifted by an angle φ with respect to the carriers in quadrature. one obtains an effective constellation rotated by an angle φ with respect to the nominal constellation P1-P4. as shown in FIG. 2A. In addition. if the frequency of oscillator **13** differs from the frequency of the carrier. angle φ increases. i.e.. the effective constellation rotates. at a speed equal to the frequency difference between the carrier and the oscillator **13**.

FIG. 2B represents the phase error variation φ when this phase difference is equal to ΔF. Signal φ is a saw-tooth varying between $-\pi/4$ and $+\pi/4$ at a frequency equal to 4ΔF

(the effective constellation reaches its nominal condition at each quarter of turn).

If the frequency difference ΔF is low (within the passband of filter **19**). the control signal of oscillator **13** follows the variation of signal φ and rapidly adjusts the frequency of oscillator **13** so that signal φ does not reach one of the limits $-\pi/4$ or $+\pi/4$. In contrast. if the frequency difference ΔF is important (much higher than the cut-off frequency of filter **19**). signal φ varies so rapidly that the control signal of oscillator **13** cannot vary at the same speed. Then. signal φ becomes a saw-tooth as represented in FIG. 2B. and the control signal of oscillator **13** establishes at the mean value. i.e. zero. of this saw-tooth signal. As a consequence. oscillator **13** is in a steady state but is set at an erroneous frequency.

To avoid this situation. lock detection circuits are used for directly analyzing signal φ and for indicating a lock condition when the amplitude of signal φ is between two thresholds. When signal φ exceeds these thresholds. oscillator **13** is forced. for example. to scan through its frequency range until a signal φ varying below these thresholds is obtained.

However. signal φ is often excessively noisy. which does not allow it to be compared with a threshold.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a detector for detecting a locked condition of a demodulator. that is efficient even if the phase error signal φ is excessively noisy.

To achieve this and other objects. the present invention provides a method for detecting a locked condition of a demodulator of at least one signal that may have discrete levels defining a constellation of nominal points in a plane. The method includes the steps of defining reference areas about the nominal points. a reference area being separated from another by a band or an angular sector crossing the origin of the constellation plane. and indicating a locked condition if the ratio of points occurring in the reference areas is above the probability for points to occur in the reference areas when the demodulator is wrongly (i.e.. incorrectly or erroneously) adjusted.

According to an embodiment of the invention. each of the reference areas is defined between two lines crossing the origin of the constellation plane.

According to an embodiment of the invention. the method is applied to QPSK demodulation. The lines are in the number of four with respective slopes of 2. ½. –½. and –2.

The invention also relates to a circuit for detecting a locked condition of a QPSK demodulator. including two absolute value circuits respectively receiving two quadrature demodulated signals; a circuit for providing the maximum and minimum values of the outputs of the two absolute value circuits; means for enabling a counter according to the sign of the difference between the maximum value and the product of the minimum value by a factor higher than 1; and means for asserting a lock indication signal when the content of the counter reaches a predetermined value.

According to an embodiment of the present invention. the counter is an up/down counter whose counting mode is selected by the sign and whose highest significant bit constitutes the lock indication signal.

The foregoing and other objects. features. aspects and advantages of the invention will become apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1. above described. schematically represents a conventional QSPK demodulator;

FIG. 2A represents, in the form of a constellation, the possible combinations of signals restored by the demodulator of FIG. 1;

FIG. 2B represents the possible variations of a phase error signal;

FIG. 3 represents an exemplary partition, according to the invention, of a constellation plane into areas having a high probability of containing an effective constellation;

FIG. 4 represents an embodiment of a lock detection circuit according to the present invention, in the exemplary case of FIG. 3; and

FIG. 5 represents an alternative element of the circuit of FIG. 4.

DETAILED DESCRIPTION

An aspect of the invention is to remark that representative points, in a constellation plane, of one or more signals restored by a demodulator, have a maximum probability to occur near points of a nominal constellation, when the demodulation oscillator **13** is suitably adjusted. When oscillator **13** is erroneously adjusted, the effective points continuously rotate from one nominal point to another, with the result that the maximum probability is not located near the nominal points but is uniformly distributed over rings including the paths of the effective points. As a result, the maximum probability for effective points to occur near the nominal points significantly decreases when the oscillator is erroneously adjusted.

To carry out lock detection, the present invention defines reference areas in which the points have a maximum probability to occur when the oscillator is suitably adjusted, and a much lower minimum probability otherwise. The number of points occurring in these areas is counted and a lock condition is detected when, in a group of occurred points, the ratio of counted points exceeds a threshold above the minimum probability. Such reference areas can be arbitrary areas surrounding the nominal points, provided that two such areas can be separated by a band or an angular sector crossing the origin of the constellation plane.

FIG. 3 represents exemplary reference areas according to the invention, for a QPSK demodulation. A first hatched area, assigned to nominal points P1 and P3, is defined between two lines DI and D2 crossing the origin of the constellation plane. A second hatched area, assigned to nominal points P2 and P4, is defined between two lines D3 and D4 crossing the origin. Lines D1–D4 have respective slopes k, 1/k, −1/k, and −k, where k is a number higher than 1.

To determine whether a point (I, Q) occurs in one of the defined reference areas, it is sufficient to ascertain the relation:

$$|I|/k<|Q|<k\,|I|,$$

or the relation:

$$\max(|I|,|Q|)-k\min(|I|,|Q|)<0.$$

Coefficient k is selected to obtain relatively narrow reference areas while ensuring a high probability for effective points to occur in these areas when the oscillator is suitably adjusted.

When k=2, the probability for points to occur in the reference areas is 0.41 when the oscillator is erroneously adjusted and close to 1 when the oscillator is suitably adjusted. The lock detection threshold is then selected at a ratio of 0.5, for example.

FIG. 4 represents an embodiment of a lock detection circuit implementing the method according to the invention described with relation to FIG. 3. This detection circuit is realized in a digital form. Actually, most of the demodulator's functions shown in FIG. 1 are frequently realized in digital form so that they are integrable at low cost.

The digital samples of signals I and Q are provided to absolute value circuits **21** and **22**, respectively. The outputs |I| and |Q| of circuits **21** and **22** are provided to a switch **24** for transmitting these outputs directly or crossed. A subtracter **26** calculates the difference between outputs |I| and |Q| and the sign sgn of this difference controls switch **24**.

With this configuration, one of the outputs of switch **24** provides the maximum value, max (|I|, |Q|) of the outputs of circuits **21** and **22**. The other output provides the minimum value min (|I|, |Q|), of the outputs of circuits **21** and **22**. A subtracter **28** calculates the difference between value max (|I|, |Q|) and value min (|I|, |Q|), previously multiplied by k by a multiplier **30**. If k=2, multiplier **30** carries out a simple wired one bit left-shift. The sign bit sgn provided by subtracter **28** is "1" when signals I and Q correspond to a point situated in one of the reference areas defined by lines D1–D4 of FIG. 3.

In order to count the number of points occurring in these reference areas, the sign bit sgn of subtracter **28** constitutes, for example, an enable signal EN for a counter **32** timed by a clock CK at the occurrence frequency of the points.

A lock indication signal LOCK is enabled when the content of counter **32** reaches a predetermined threshold. Signal LOCK corresponds, for example, to the most significant bit Qn of the counter. Counter **32** is periodically reset by a signal RST having a frequency significantly lower than the occurrence frequency of the points, for example 1000 times lower, so as to analyze sufficiently representative groups of points.

FIG. 5 illustrates a second approach for detecting a lock condition in the case where the detection threshold is set to a ratio of 0.5. An up/down counter **36** timed by clock CK replaces the counter **32** of FIG. 4. The enable signal EN selects its up-counting mode by level 1 and its down-counting mode by level 0.

With this configuration, the up/down counter **36** accumulates the difference between the number of valid points occurring in the reference areas and the number of non-valid points occurring outside the reference areas. If the average number of valid points is higher than the average number of non-valid points, the content of the up/down counter increases until it reaches its upper limit. The lock indication signal LOCK is provided, for example, by the most significant bit Qn of the up/down counter. The time needed to reach this upper limit, and therefore the number of points for which the difference is accumulated, vary as a function of the number of bits of the up/down counter and of the adjustment error of the oscillator. The number of bits of the up/down counter **36** is selected so that the difference is accumulated for a sufficiently representative group of points. In the example of FIG. 3, an 8-bit up/down counter can be chosen.

The up/down counter is preferably connected so as to saturate instead of overflowing, i.e., when it reaches its upper or lower limit without the counting mode being changed, an additional clock pulse no longer changes the state of the up/down counter.

The reference areas defined by lines as in FIG. 3 enable the realization of a very simple lock detector. Of course, these reference areas can be defined by other geometric figures, such as circles centered on the nominal points.

The circuit of FIG. 4 can be used to obtain, in addition to lock detection, useful values for the demodulator, such as the